

INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)			ATTY DOCKET NO. BUR920030019US1		SERIAL NO. <i>10/604,225</i>	
			FILING <i>7-1-03</i>		GROUP <i>6811 UNKNOWN</i>	
PATENT & TRADEMARKS. PATENT DOCUMENTS						
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS
FILING DATE IF APPROPRIATE						
<i>[A large grid of 10 rows by 4 columns for listing patent documents, with a diagonal line drawn through it.]</i>						
FOREIGN PATENT DOCUMENTS						
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS
TRANSLATION						
YES NO						
<i>[A large grid of 10 rows by 4 columns for listing foreign patent documents, with a diagonal line drawn through it.]</i>						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)						
<i>RHO</i>		International Business Machines Corporation, "Hybrid Transistional Coding of Wide On-Chip Busses", Research Disclosure, Nov. 2001, pp. 1958-1959.				
<i>RHO</i>		Nalamalpu et al., "Boosters For Driving Long Onchip Interconnects-Design Issues, Interconnect Synthesis, and Comparison with Repeaters", IEEE Xplore, Vol. 21, No. 1, January 2002, pp. 50-62.				
EXAMINER	<i>Rompha L. Owen</i>		DATE CONSIDERED		<i>1/26/06</i>	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						

INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		PCT/US JUL 17 2003 RECEIVED U.S. PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. BUR920030019US1		SERIAL NO. 10/604205	
				S: FILING	7-1-03	GROUP 281 Unknown	
PATENT & TRADEMARK DOCUMENTS							
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
<i>DKG</i>		Yamada et al., "A Novel Approach to Realizing Flexible Transport Systems Using Reconfigurable Hardware", IEEE, Vol. 1, November 1995, pp. 67-71.					
EXAMINER		<i>Douglas K. Owen</i>		DATE CONSIDERED		<i>1/26/06</i>	

***EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

07/01/03

Title of Invention

CIRCUIT AND METHOD FOR PIPELINED INSERTION

Application Number :

10/604205

Confirmation Number:

First Named Applicant: Robert Horton

Attorney Docket Number: BUR920030019US1

Art Unit: 2811

Examiner: Owens

Search string: (5369640 or 5930525 or 6018782 or 6035364 or 6275975 or 6279142 or 6415344 or 6426656 or 20020161959 or 20020175390).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
qv	1	5369640	1994-11-29	Watson et al.			
qv	2	5930525	1999-07-27	Gotesman et al.			
qv	3	6018782	2000-01-25	Hartmann			
qv	4	6035364	2000-03-07	Lambrecht et al.			
qv	5	6275975	2001-08-14	Lambrecht et al.			
qv	6	6279142	2001-08-21	Bowen et al.			
qv	7	6415344	2002-07-02	Jones et al.			
qv	8	6426656	2002-07-30	Dally et al.			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
qv	1	20020161959	2002-10-31	Apostol, Jr. et al.			
qv	2	20020175390	2002-11-21	Craft			

Signature

Examiner Name	Date
(Signature)	05/14/04